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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

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Application Number	09/888,002
Filing Date	June 21, 2001
First Named Inventor	Whonchee Lee
Art Unit	3723,
Examiner Name	Dung V. Nguyen
Confirmation Number	9049
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This is a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant applications filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. § 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
     - iii. ☐ Other
   - b. ☒ Enclosed
     - i. ☐ Amendment/Reply
     - ii ☐ Affidavit(s)/Declaration(s)
     - iii. ☒ Information Disclosure Statement (IDS)
     - iv. ☒ Other: Cited References (4); Check

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2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) required)
   - b. ☐ Other

3. Fees — The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0665
     - i. ☐ RCE fee required under 37 C.F.R. 1.17(e)
     - ii. ☐ Extension of time fee (37 C.F.R. 1.136 and 1.17)
     - iii. ☒ Other: any underpayment

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   - b. ☒ Check in the amount of $ 750 enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Name (Print/Type)	John M. Wechkin	*Registration No. (Attorney/Agent)*	42,216
Signature		*Date*	August 7, 2003

CERTIFICATE OF MAILING OR TRANSMISSION

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CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of a semiconductor device characterized by providing the following. The process which forms the slot for wiring for forming wiring in the insulator layer formed on the substrate. The process which makes a metal membrane deposit on the aforementioned insulator layer so that the aforementioned slot for wiring may be embedded. The process which forms the passive state film which demonstrates the operation which bars the electrolysis reaction of the metal membrane concerned in the front face of the metal membrane deposited on the aforementioned insulator layer. The process which carries out flattening of the irregularity of the front face of the aforementioned metal membrane which removed alternatively the immobility film on the heights which exist in the front face of the aforementioned metal membrane produced by the embedding of the aforementioned slot for wiring among the passive state films formed in the aforementioned metal membrane by mechanical polishing, removed the process which exposes the heights of the metal concerned on a front face, and the heights of the metal membrane which carried out [aforementioned] exposure by electrolytic polishing, and produced by the embedding of the aforementioned slot for wiring.

[Claim 2] the electrolysis compound polish which compounded electrolytic polishing and mechanical polishing for the excessive metal membrane to which the aforementioned front face exists on the aforementioned insulator layer of the metal membrane by which flattening was carried out -- the manufacture method of a semiconductor device according to claim 1 of having further the process which removes and forms the aforementioned wiring

[Claim 3] The aforementioned electrolysis compound polish is the manufacture method of a semiconductor device according to claim 2 of compounding electrolytic polishing and chemical machinery polish.

[Claim 4] The manufacture method of a semiconductor device according to claim 2 characterized by providing the following. After forming the aforementioned slot for wiring, the barrier film which consists of a conductive material for preventing the diffusion to the aforementioned insulator layer of the aforementioned metal membrane so that the aforementioned insulator layer top and aforementioned Mizouchi may be covered forms. The process remove until the aforementioned barrier film exposes the excessive metal membrane which exists on the aforementioned insulator layer to a front face by the aforementioned electrolysis compound polish, after carrying out flattening in the heights of the metal membrane which carried out [aforementioned] exposure. The process removed by the aforementioned electrolysis compound polish until the aforementioned insulator layer exposes to a front face the excessive barrier film which exists on the aforementioned insulator layer.

[Claim 5] Make the electrolytic solution intervene between the polished surface of the abrasive tools which have conductivity, and the aforementioned passive state film, use the aforementioned metal membrane and a barrier film as an anode plate, and the aforementioned abrasive tools are used as cathode. Impress voltage between the aforementioned metal membrane and a barrier film, and the aforementioned abrasive tools, and the aforementioned abrasive tools are moved to it relatively [front face / of the aforementioned passive state film]. The manufacture method of a semiconductor device according to claim 4 of making the heights of the aforementioned metal membrane exposed from the passive state film which removed alternatively the passive state film formed in the heights of the aforementioned metal membrane, and was removed by the aforementioned selection target eluted by the electrolytic action of the aforementioned electrolytic solution.

[Claim 6] The manufacture method of a semiconductor device according to claim 5 of making the polar-zone material to which voltage was impressed between the aforementioned abrasive tools contacting or approaching the aforementioned metal membrane and a barrier film, energizing on the aforementioned metal membrane and the aforementioned barrier film, carrying out the monitoring of the current which flows from the aforementioned polar-zone material to the aforementioned abrasive tools via the aforementioned aforementioned metal membrane and the aforementioned barrier film, and managing advance of polish of the aforementioned metal membrane and a barrier film based on the size of the current value concerned.

[Claim 7] The manufacture method of a semiconductor device according to claim 5 of making the polar-zone material to which voltage was impressed between the aforementioned abrasive tools contacting or approaching the aforementioned metal membrane and a barrier film, energizing on the aforementioned metal membrane and the aforementioned barrier film, carrying out the monitoring of the size of the electric resistance generated between the aforementioned polar-zone material and the aforementioned abrasive tools, and managing advance of polish of the aforementioned metal membrane and a barrier film based on the electric resistance value concerned.

[Claim 8] The manufacture method of a semiconductor device according to claim 5 of making the chemical-polishing agent containing a polish abrasive grain intervening between the polished surface of the aforementioned abrasive tools, and the aforementioned passive state film, and removing the aforementioned passive state film alternatively.

[Claim 9] each material which constitutes the aforementioned metal membrane and the aforementioned barrier film -- receiving -- a different chemical-polishing agent with a respectively high polish rate -- using -- the above -- the manufacture method of a semiconductor device according to claim 5 of removing an excessive metal membrane and a barrier film, respectively

[Claim 10] the above -- the voltage impressed between the aforementioned barrier film and the aforementioned abrasive tools at the process which removes an excessive barrier film -- the above -- the manufacture method of the semiconductor device according to claim 5 made lower than the voltage impressed between the aforementioned metal membranes in a process and the aforementioned abrasive tools which remove an excessive metal membrane

[Claim 11] The process which the process which forms the aforementioned slot for wiring has the process which forms the contact hole for connecting the impurity-diffusion layer or the wiring formed in the lower layer of the aforementioned insulator layer, and the wiring formed on the insulator layer concerned, and embeds in a metal to the aforementioned slot for wiring with formation of the aforementioned slot for wiring is the manufacture method of a semiconductor device according to claim 2 of embedding a metal to the aforementioned contact hole with the aforementioned slot for wiring.

[Claim 12] The manufacture method of the semiconductor device according to claim 11 which uses copper for the formation material of the aforementioned wiring, and embeds copper at the aforementioned slot for wiring, and a contact hole using an electroplating method.

[Claim 13] The manufacture method of a semiconductor device according to claim 4 of using either Ta, Ti, TaN and TiN for the formation material of the aforementioned barrier film.